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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

FAULK, DEVONA E

ART UNIT	PAPER NUMBER
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2644

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/362,941

Applicant(s)

KAMIYA ET AL.

Examiner

Devona E. Faulk

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 July 1999.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1,11,12,14,16 and 18** are rejected under 35 U.S.C. 102(b) as being anticipated by Kuribayashi et al. (U.S. Patent 5,539,145).

Regarding **claim 1**, Kuribayashi discloses a tone data recording and reproducing device comprising a fetch buffer memory (XBUFA, XBUFB) that temporarily stores tone data read out from the hard disk (HD). The HD is a mass storage device. The fetch buffer reads on “an input buffer for storing the waveform sample data received from said storage device”; a reproduction buffer memory (PBUFA, PBUFB) from which the reproduced sound generation circuit reads out the tone data stored, which reads on “output buffer”; a reproduction/transfer control section (PD) that which determines in which mode the reproduction process should be done (column 15, line 24-25) (column 17, line-16- column 23) which reads on “a processor connected with the input buffer and said output buffer and adapted to execute” ; a reproduced sound generation circuit (TG) that reads out the tone data stored in the reproduction buffer memory (PBUFA, PBUFB) at a predetermined reproductive readout rate and in accordance with predetermined reproduction sampling clock pulses (column 9, lines 5-13) (column 8, lines 24-37) which reads on “a first reading process for reading out the waveform sample data stored in said input buffer and converting the sampling rate of the read-out waveform sample data to an inner sampling rate

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selected from among a plurality of predetermined inner sampling rates”; a re-sampling circuit (21) that re-samples tone waveform sample data to be given from the A/D converter to the record buffer memory (RBUFA, RBUFB), which reads on “a second process for performing predetermined arithmetic processing on the waveform sample data converted to the selected inner sampling rate”; and a D/A converter (22) (Figure 2), connected to the re-sampling circuit (21), which reads on “a third process for converting the waveform sample data having undergone the predetermined arithmetic processing to a predetermined output sampling rate”. Figure 2 indicates that data can bi-directional between the reproduced sound generation circuit (TG) and the reproduction/transfer control section, which reads on “a fourth process for writing, into said output buffer, the waveform data converted to the predetermined output sampling rate”.

Regarding **claim 11**, Kuribayashi teaches of determining the pitch of the waveform that is read out at sampling timings according to the predetermined reproduction sampling frequency (column 9, line25-32), which reads on the claimed matter.

3. Regarding **claim 12**, Kuribayashi discloses a tone data recording and reproducing device comprising a CPU (10), which reads on “a central processing unit”; a hard disk (HD) (Figure 2) (column 6, lines 63-column 7), which reads on “a storage device storing waveform sample data sampled at a given sampling rate and connected via a bus to said central processing unit”; a record/reproduction device (RU) (Figure 2) that reads on the “tone data processing device” as claimed; a fetch buffer memory (XBUFA, XBUFB) that temporarily stores tone data read out from the hard disk (HD). The HD is a mass storage device. The fetch buffer reads on “an input buffer for storing the waveform sample data received from said storage device”; a reproduction buffer memory (PBUFA, PBUFB) from which the reproduced sound generation circuit reads out

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the tone data stored, which reads on “output buffer”; a reproduction/transfer control section (PD) that which determines in which mode the reproduction process should be done (column 15, line 24-25) (column 17, line 16- column23) which reads on “a processor connected with the input buffer and said output buffer and adapted to execute” ; a reproduced sound generation circuit (TG) that reads out the tone data stored in the reproduction buffer memory (PBUFA, PBUFB) at a predetermined reproductive readout rate and in accordance with predetermined reproduction sampling clock pulses (column 9, lines 5-13) (column 8, lines 24-37) which reads on “a first reading process for reading out the waveform sample data stored in said input buffer and converting the sampling rate of the read-out waveform sample data to an inner sampling rate selected from among a plurality of predetermined inner sampling rates”; a re-sampling circuit (21) that resamples tone waveform sample data to be given from the A/D converter to the record buffer memory (RBUFA, RBUFB), which reads on “ a second process for performing predetermined arithmetic processing on the waveform sample data converted to the selected inner sampling rate” ; and a D/A converter (22) (Figure 2), connected to the re-sampling circuit (21), which reads on “a third process for converting the waveform sample data having undergone the predetermined arithmetic processing to a predetermined output sampling rate” . Figure 2 indicates that data can bi-directional between the reproduced sound generation circuit (TG) and the reproduction/transfer control section, which reads on “a fourth process for writing, into said output buffer, the waveform data converted to the predetermined output sampling rate”.

4. Regarding **claim 14**, Kuribayashi discloses a tone data recording and reproducing device comprising a reproduced sound generation circuit (TG) that reads out the tone data stored in the reproduction buffer memory (PBUFA, PBUFB) at a predetermined reproductive readout rate and

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in accordance with predetermined reproduction sampling clock pulses (column 9, lines 5-13) (column 8, lines 24-37) which reads on “a first step of reading out the waveform sample data stored in said input buffer and converting the sampling rate of the read-out waveform sample data to an inner sampling rate selected from among a plurality of predetermined inner sampling rates”; a re-sampling circuit (21) that resamples tone waveform sample data to be given from the A/D converter to the record buffer memory (RBUFA, RBUFB), which reads on “ a second step of performing predetermined arithmetic processing on the waveform sample data converted to the selected inner sampling rate” ; and a D/A converter (22) (Figure 2), connected to the re-sampling circuit (21), which reads on “a third step of converting the waveform sample data having undergone the predetermined arithmetic processing to a predetermined output sampling rate” . Figure 2 indicates that data can bi-directional between the reproduced sound generation circuit (TG) and the reproduction/transfer control section, which reads on “a step of writing, into said output buffer, the waveform data converted to the predetermined output sampling rate”. Kuraibayashi teaches that a PC is employed as a host control device. Therefore, there is inherently some type of machine-readable medium that executes the process.

5. Regarding **claim 16**, Kuribayashi discloses a tone data recording and-reproducing device comprising a reproduced sound generation circuit (TG) that reads out the tone data stored in the reproduction buffer memory (PBUFA, PBUFB) at a predetermined reproductive readout rate and in accordance with predetermined reproduction sampling clock pulses (column 9, lines 5-13) (column 8, lines 24-37) which reads on “a first sampling rate conversion section for converting the sampling rate of the received waveform sample data to an inner sampling rate selected from among a plurality of predetermined inner sampling rates” and “wherein tone data is generated in

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accordance with the predetermined output sampling rate”; a re-sampling circuit (21) that re-samples tone waveform sample data to be given from the A/D converter to the record buffer memory (RBUFA, RBUFB), which reads on “ an arithmetic processing section for performing predetermined arithmetic processing on the waveform sample data converted to the selected inner sampling rate” ; and a D/A converter (22) (Figure 2), connected to the re-sampling circuit (21), which reads on “a second sampling rate conversion section for converting the waveform sample data having undergone the predetermined arithmetic processing to a predetermined output sampling rate” .

6. Regarding **claim 18**, Kuribayashi discloses a tone data recording and reproducing device comprising a reproduced sound generation circuit (TG) that reads out the tone data stored in the reproduction buffer memory (PBUFA, PBUFB) at a predetermined reproductive readout rate and in accordance with predetermined reproduction sampling clock pulses (column 9, lines 5-13) (column 8, lines 24-37) which reads on “a step of converting the sampling rate of the received waveform sample data to an inner sampling rate selected from among a plurality of predetermined inner sampling rates” and “wherein tone data is generated in accordance with the predetermined output sampling rate”; a re-sampling circuit (21) that resamples tone waveform sample data to be given from the A/D converter to the record buffer memory (RBUFA, RBUFB), which reads on “ a step of performing predetermined arithmetic processing on the waveform sample data converted to the selected inner sampling rate” ; and a D/A converter (22) (Figure 2), connected to the re-sampling circuit (21), which reads on “a step of converting the waveform sample data having undergone the predetermined arithmetic processing to a predetermined output sampling rate” .

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. **Claim 2-8, 13,15 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuribayashi (U.S. Patent 5,539,145).

Regarding **claim 2**, Kuribayashi further teaches of one aspect of the invention that includes a readout section for sequentially reading out the waveform data stored in the second storage section. Thus the concept of sequentially reading out data from a buffer was well known in the art at the time of filing. It is a matter of design choice as to how the output frequency would correspond to another sampling rate. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kuribayashi's apparatus such that the waveform data is read out sequentially as claimed for the benefit of having the capability reproducing a generated tone.

Regarding **claim 3**, Kuribayashi teaches that the record/reproduction device (RU) prepares address signals synchronous with the write or readout operation with respect to the storage area and controls the supply of tone data to be recorded into the hard disk (HD) in accordance with the address signals or controls the fetch of tone data read out from the hard disk (HD) (column 7, lines 23-28). It is a matter of design choice whether to receive data at equal periods or not. Thus it would have been obvious to one of ordinary skill in the art at the time of

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the invention to modify Kuribayashi's device to receive data from the storage device as claimed for the benefit of having a more flexible device.

Regarding **claim 4**, it is a matter of design choice as to how a sampling rate is selected, and if one sampling rate is converted to another. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kuribayashi's device so that a predetermined sampling rate is selected as claimed for the benefit of meeting design specifications.

Regarding **claim 5**, Kuribayashi further teaches that the buffer memories (XBUFA,XBUFB,PBUFA,PBUFB,RBUFA,RBUFB) is composed of two memory sections and that write to and readout from each of the buffer memories can be simultaneously done in a parallel manner (column 10, lines 15-22). He further teaches that the buffer memories can be formatted into more than two memories, each representative of a different channel (Figure 10). Kuribayashi further teaches of one aspect of the invention that includes a readout section for sequentially reading out the waveform data stored in the second storage section. Thus the concept of sequentially reading out data from a buffer was well known in the art at the time of filing. It is a matter of design choice as to how the output frequency would correspond to another sampling rate. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kuribayashi's apparatus such that the waveform data is read out sequentially as claimed for the benefit of having the capability reproducing a generated tone.

Regarding **claim 6**, Kuribayashi further teaches that the record sampling frequency for channels may be different. Kuribayashi's device has the capability of simultaneously reproducing plural sound recorded with different sampling frequencies, in accordance with a

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common reproduction sampling frequency column 24, lines 1-67). He further teaches that the PC is capable of designating a sampling frequency and performing processing on the waveform sample data of different channels as claimed (column 12, lines 66-67) column 25, lines 40-column 26-column 30). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use Kuribayashi's device for the benefit of giving the device the capability to reproducing sounds have different sampling frequencies.

Regarding **claim 7**, Kuribayashi discloses a tone data recording and reproducing device comprising a CPU (10), which reads on "a central processing unit"; a hard disk (HD) (Figure 2) (column 6, lines 63-column 7), which reads on "a storage device storing waveform sample data sampled at a given sampling rate and connected via a bus to said central processing unit"; a record/reproduction control device (RU) (Figure 2) that reads on the "tone data processing device" as claimed. Thus it would have been obvious to use Kuribayashi's apparatus for the benefit of minimizing the processing burden on the host control device or the computer.

Regarding **claim 8**, it is a matter of design choice as to how the sampling is done. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kuribayashi's device as claimed for the benefit of meeting design specifications.

Regarding **claims 13 and 15**, Kuribayashi further teaches of one aspect of the invention that includes a readout section for sequentially reading out the waveform data stored in the second storage section. Thus the concept of sequentially reading out data from a buffer was well known in the art at the time of filing. It is a matter of design choice as to how the output frequency would correspond to another sampling rate. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kuribayashi's apparatus such that

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the waveform data is read out sequentially as claimed for the benefit of apparatus such that the waveform data is read out sequentially as claimed for the benefit of having the capability reproducing a generated tone.

Regarding **claim 17**, it is a matter of design choice as to how a sampling rate is selected, and if one sampling rate is converted to another. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kuribayashi's device so that a predetermined sampling rate is selected as claimed for the benefit of having a device designed as chosen by the designer of the device.

8. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuribayashi (U.S. Patent 5,539,145) in view Hideo (U.S. Patent 5,532,424).

Regarding **claim 9**, Hideo teaches of generating samples using a filter means and resolution of coefficients in accordance with each sampling clock (See abstract) (column 3, 45-55) (column 8, line 46-56) (Figure 1). It would be a matter of design choice as to whether or not the coefficients are changed in accordance with the selected inner sampling rate. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kuribayashi's device to use Hideo's filter means and resolution of coefficient means for the benefit of having a device capable of canceling undesirable frequency characteristics imparted to a tone signal.

9. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuribayashi (U.S. Patent 5,539,145) in view of Mitsuhashi et al. (U.S. Patent 5,127,306).

Regarding **claim 10**, Mitsuhashi discloses an apparatus for applying panning effects to musical tone signals (Figure 4) that includes filters (1-13, 4-2,4-1), an amplifier (1-14), an adder

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circuit (4-7) where signals are mixed (column 10, line 26-column 11, line 38). Thus it would have been obvious to one of ordinary skill in the art to modify Kuribayashi's device by incorporating Mitsuhashi's panning effects apparatus for the benefit of applying an independent automatic panning effect on each group of musical tones for more variety of musical-tone expressions.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devona E. Faulk whose telephone number is 703-305-4359. The examiner can normally be reached on 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W. Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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XU MEI
PRIMARY EXAMINER